

### **Amendment to Claims**

Please cancel claims 11-33, 35-37 and 40-46.

1. (Original) A structure for containing desiccant in at least one of a wafer level packaged device and a die level packaged device, the structure comprising:

    a substrate;

    a first metal layer disposed on the substrate within a predetermined area;

    a second metal layer defining the predetermined area;

    a dielectric layer disposed on the first metal layer;

    a desiccant disposed on the dielectric layer;

    a permeable membrane disposed on the desiccant and the dielectric layer, wherein the permeable membrane surrounds the desiccant, the dielectric layer, and the first metal layer, and is within the predetermined area; and

    a plurality of metal traces disposed on the permeable membrane.

2. (Original) The structure as defined in claim 1 wherein the substrate is at least one of single crystal silicon, polycrystalline silicon, silicon oxide containing dielectric substrates, alumina, sapphire, ceramic, glass, silicon wafers, germanium wafers, gallium arsenide wafers, and mixtures thereof.

3. (Original) The structure as defined in claim 1 wherein the first metal layer, the second metal layer, and the metal traces are held substantially equi-potential to a potential of at least one of the wafer and the die.

4. (Original) The structure as defined in claim 1 wherein the first metal layer is at least one of gold, aluminum, tantalum, platinum, iridium, palladium, rhodium, nickel chromide, doped polysilicon, and mixtures thereof.

5. (Original) The structure as defined in claim 1 wherein the second metal layer is at least one of gold, aluminum, tantalum, platinum, iridium, palladium, rhodium, nickel chromide, doped polysilicon, and mixtures thereof.

6. (Original) The structure as defined in claim 1 wherein the plurality of metal traces is at least one of gold, tantalum, aluminum, platinum, iridium, palladium, rhodium, nickel chromide, and mixtures thereof.

7. (Original) The structure as defined in claim 1 wherein the dielectric layer comprises at least one of silicon oxide and silicon nitride.

8. (Original) The structure as defined in claim 1 wherein the permeable membrane comprises at least one of a polymeric material and a porous ceramic material.

9. (Original) The structure as defined in claim 8 wherein the polymeric material is a flexible material.

10. (Original) The structure as defined in claim 1 wherein the desiccant is at least one of silica gel, calcium oxide, calcium sulfate, and molecular sieves.

Claims 11-33. (Cancelled.)

34. (Original) An integrated circuit, comprising:

a hermetically sealed area having the integrated circuit operatively disposed therein; and

a structure within the hermetically sealed area for containing a desiccant, the structure comprising:

a substrate;

a first metal layer disposed on the substrate within a predetermined area;

a second metal layer defining the predetermined area;

a dielectric layer disposed on the first metal layer;

a desiccant disposed on the dielectric layer;

a permeable membrane disposed on the desiccant and the dielectric layer, wherein the permeable membrane surrounds the desiccant, the dielectric layer, and the first metal layer, and is within the predetermined area; and

a plurality of metal traces disposed on the permeable membrane.

Claims 35-37 (Cancelled).

38. (Original) A structure for containing desiccant in at least one of a wafer level packaged device and a die level packaged device, the structure comprising:

a substrate;

a metal layer disposed on the substrate;  
    a dielectric layer disposed on the metal layer;  
    a desiccant disposed on the dielectric layer;  
    a permeable membrane disposed on the desiccant and the dielectric layer, wherein  
the permeable membrane surrounds the desiccant, the dielectric layer, and the metal  
layer; and  
    a plurality of metal traces disposed on the permeable membrane.

39. (Original) The structure as defined in claim 38 wherein the metal layer  
and the metal traces are held substantially equi-potential to a potential of at least one of  
the wafer and the die.

Claims 40-46 (Cancelled).